**IN THE CLAIMS**

Claim 1 (Currently Amended) A method comprising:

selecting a phase threshold value,

receiving a plurality of ~~sequenced~~ branch trace buffers in sequence, the plurality of branch trace buffers including a plurality of branch addresses,

determining a plurality of branch address vectors from the plurality of branch addresses,

determining histogram bins from the plurality of branch address vectors,

determining a distance between centers of at least two consecutive histogram bins,

comparing the distance with said selected threshold value, ~~and~~

determining major execution phases of an executable process based on the comparison, and

using the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment.

Claim 2 (Currently Amended) The method of claim 1, said plurality of ~~sequenced~~ trace buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.

Claim 3 (Canceled)

Claim 4 (Currently Amended) The method of claim 1, where a result of said determining major execution phases ~~to signal a requisite~~is used for dynamically compiling executable code to optimize said executable code.

Claims 5-6 (Canceled)

Claim 7 (Currently Amended) An apparatus comprising a machine-readable medium containing instructions which, when executed ~~by~~ cause a machine~~, cause the machine~~ to ~~perform operations comprising~~:

~~selecting~~ select a phase threshold value,

~~receiving~~ receive a plurality of branch trace ~~sequenced~~ buffers in sequence, the plurality of branch trace buffers including a plurality of branch addresses,

determine a plurality of branch address vectors from the plurality of branch addresses,

~~determining~~ determine histogram bins from the ~~a~~ plurality of branch addresses vectors ~~representing a branch trace buffer~~,

~~determining~~ determine a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, ~~and~~

~~comparing~~ compare the distance with said selected threshold value,

determine major execution phases of an executable process based on a result of the compare, and

use the determined major execution phases for determining where compiler optimization is needed to improve performance in a managed run-time environment.

Claim 8 (Canceled)

Claim 9 (Currently Amended) The apparatus of claim 8, wherein said ~~determining~~ determine major execution phases is dynamic at a predetermined periodic rate.

Claim 10 (Currently Amended) The apparatus of claim 8, wherein said ~~determining~~ determine major execution phases is manually commenced.

Claim 11 (Currently Amended) The apparatus of claim 7, said plurality of ~~sequenced~~ branch trace buffers in sequence comprising samples containing addresses of a plurality of branches taken at a sampling time.

Claim 12 (Currently Amended) The apparatus of claim 7, where a result of said ~~determining~~ determine major execution phases instruction ~~to signal a requisite~~is used for dynamically compiling executable code to optimize said executable code.

Claims 13-14 (Canceled)

Claim 15 (Currently Amended) A system comprising:

a processor coupled to one of a main memory and a cache memory,

at least one process to communicate with said memory, and ~~a~~

a phase detector that operates to determine major execution phases of said at least one process to determine where compiler optimization is needed to improve performance of the at least one process in a managed run-time environment.

Claim 16 (Canceled)

Claim 17 (Currently Amended) The system of claim 15, said phase detector including a receiver toreceive a plurality of ~~sequenced~~ trace buffers in sequence, the plurality of branch trace buffers including a plurality of branch addresses,

~~wherein~~ said phase detector operates to determine a plurality of branch addresses ~~vectorsrepresenting a branch trace buffer~~,

determine histogram bins from the plurality of branch address vectors,

determine a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, and

compare the distance with a predetermined threshold value.

Claim 18 (Currently Amended) The system of claim 17, said phase detector having logic to:

determine a plurality of consecutive branch addresses representing ~~the~~ a branch trace buffer,

determine a stable phase histogram for ~~the~~ a plurality of consecutive branch addresses, and

determine a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses.

Claim 19 (Original) The system of claim 15, wherein said phase detector having logic to determine major execution phases dynamically at a predetermined periodic rate.

Claim 20 (Original) The system of claim 17, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.

Claim 21 (Currently Amended) A system comprising:

a first device having a first processor coupled to a first memory and at least one process to communicate with said first memory, and

a second device having a second processor coupled to a second memory and at least another process to communicate with said second memory,

wherein a phase detector process operating in one of said first processor and said second processor operate to determine major execution phases of one of said one process and said another process within one of said first device and said second device for determining where compiler optimization is needed for one of said one process and said another process to improve performance in a managed run-time environment.

Claim 22 (Canceled)

Claim 23 (Currently Amended) The system of claim 21, said phase detector having logic to:

receive a plurality of ~~sequenced~~ trace buffers in sequence, the plurality of trace buffers including a plurality of branch addresses,

determine a plurality of branch addresses vectors ~~representing a branch trace buffer~~,

determine histogram bins from the plurality of branch address vectors,

determine a distance between centers of at least two consecutive histogram bins, where said at least two histogram bins are non-overlapping, and

compare the distance with a predetermined threshold value.

Claim 24 (Currently Amended) The system of claim 23, said phase detector having logic to:

determine a plurality of consecutive branch addresses representing ~~the~~ a branch trace buffer,

determine a stable phase histogram for the plurality of consecutive branch addresses, and

determine a plurality of equally spaced and non-overlapping histogram bins for all possible branch addresses.

Claim 25 (Original) The system of claim 21, wherein said phase detector having logic to determine major execution phases dynamically at a predetermined periodic rate.

Claim 26 (Original) The system of claim 23, said plurality of sequenced buffers comprising samples containing addresses of a plurality of branches taken at a sampling time.